Amendments to the Claims:

This listing of claims replaces all prior versions and listings of claims in the application:

Listing of Claims:

1-5. (Cancelled)

6. (Currently Amended) A system comprising:

a bus; and

a digital signal processor comprising:

a multiplier having a first structure and a second structure, the first structure processing data up to n-bits and the second structure processing data up to (n/2)-bits; and

a data size selector which configures the multiplier into the first structure of a single n-bit multiplier when the data is greater than (n/2)-bits and configures the multiplier into the second structure of two (n/2)-bit multipliers when the data is (n/2)-bits or less.

7 - 8. (Cancelled)

9. (Original) The system of Claim 6, further comprising a plurality of arithmetic logic units to collect the processed data.

10. (Original) The system of Claim 6, further comprising a flop which stores the result of the multiplier.

11. (Original) The system of Claim 10, further comprising at least one arithmetic logic unit which adds the result from the multiplier to a running total.

12. (Original) A method comprising:

determining a size of data to be processed;

configuring a first processing path for data of n-bits if the data size is greater than (n/m)-bits; and

dividing the first processing path into multiple processing paths if the data size is (n/m)-bits or less.

13. (Original) The method of Claim 12, further comprising configuring each of the multiple processing paths for data sizes smaller than the first processing path.

14. (Original) The method of Claim 12, further comprising dividing the first processing path into m processing paths.

15. (Original) The method of Claim 12, further comprising including an n-bit multiplier in the first processing path.

16. (Original) The method of Claim 12, further comprising defining m=2.